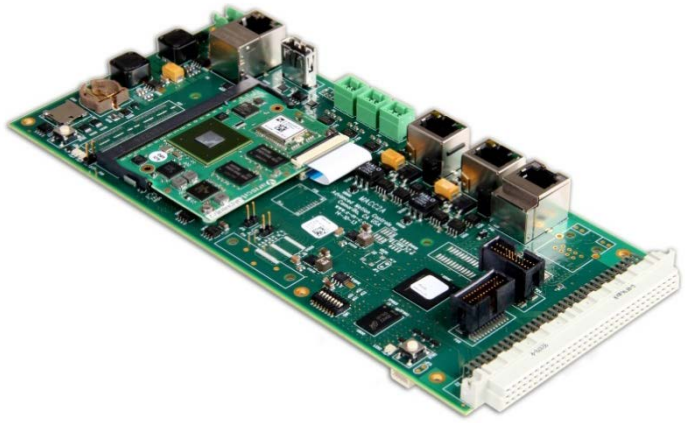
Description

The Motion Automation Control Card (MACC) family are general purpose motion/automation controllers with embedded Click&Move® programming capability.

The MACC02 is a stand-alone card operating off a nominal 24 VDC power supply that can control a network of *ADVANCED* Motion Controls®' DigiFlex® Performance™ digital servo drives as well as non-networked *ADVANCED* Motion Controls®' analog or digital drives. An optional plug-in I/O module with dedicated and user-defined digital and analog I/O provides additional I/O points through the MACC02's FPGA.

A Click&Move® user program can be developed, compiled and tested on a PC and recompiled for the MACC platform. Once downloaded into the MACC02, it can be debugged, controlled, and monitored in real-time via an Ethernet UDP/IP connection by a PC with a client Click&Move® application.

Click&Move® user programs can also be distributed between the PC and the MACC02; the fast, time-critical portion of the application can run in the MACC02 while Click&Move®'s HMI less time-critical portions run in the PC.



Click&Move®
Automation Solution

Features

- Uses On-Board High Performance System On Module with ARM Cortex-A9 Microprocessor Operating with Real-Time Linux
- Fits Standard DIN Rail Plastic Case
- External I/O Module Connectivity
- Fully Functional PLC Utilizing Click&Move® Programmability and I/O Modules
- Servo Drive and I/O Command Update Rates Down to the 50-100µs Range
- Two Galvanically Isolated CAN Interfaces
- Directly Integrates CANopen, EtherCAT®, or Ethernet Powerlink Field Bus Masters
- Compatible with *ADVANCED* Motion Controls®' DxM™ Technology
- Drive Communication via RS232
- USB 2.0 and USB 2.0 OTG Connectivity for High and Full Speed Devices
- WLAN and Bluetooth Compatible
- Micro SD Card Slot
- Surface-Mount Battery Holder for Optional On-Board Clock Supply
- Display, Camera, PCIe, SATA, Audio Interfaces
- Optional HDMI Connector

ADVANCED MOTION CONTROLS®' DRIVE COMPATIBILITY

- DigiFlex® Performance™ Digital Servo Drives
- Torque or Velocity Mode Analog Servo Drives

NETWORK COMMUNICATION TYPES

- CANopen
- EtherCAT®
- Ethernet Powerlink
- RS232

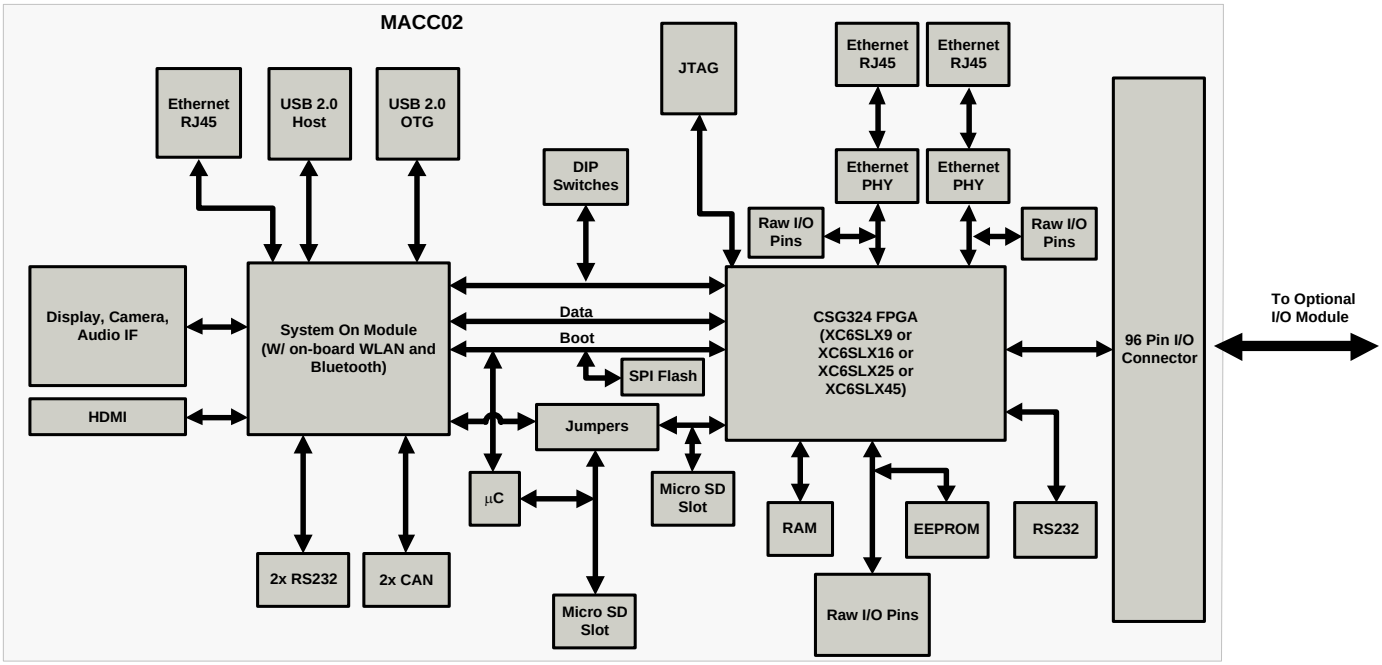
FPGA SUBSYSTEM

- Spartan®-6 FPGA
- User-defined I^2C EEPROM
- 32 to 256 MB DDR2 RAM
- Up to 132 Raw FPGA I/O Pins Available
- UART Interface to System On Module
- Optional On-Board SPI Configuration FLASH
- Up to Two Dedicated 10/100TX Ethernet PHY
- Direct Access to Micro SD Slot
- Optional Boot from the SD Card

COMPLIANCES & AGENCY APPROVALS

- UL/cUL Pending
- CE Pending
- RoHS

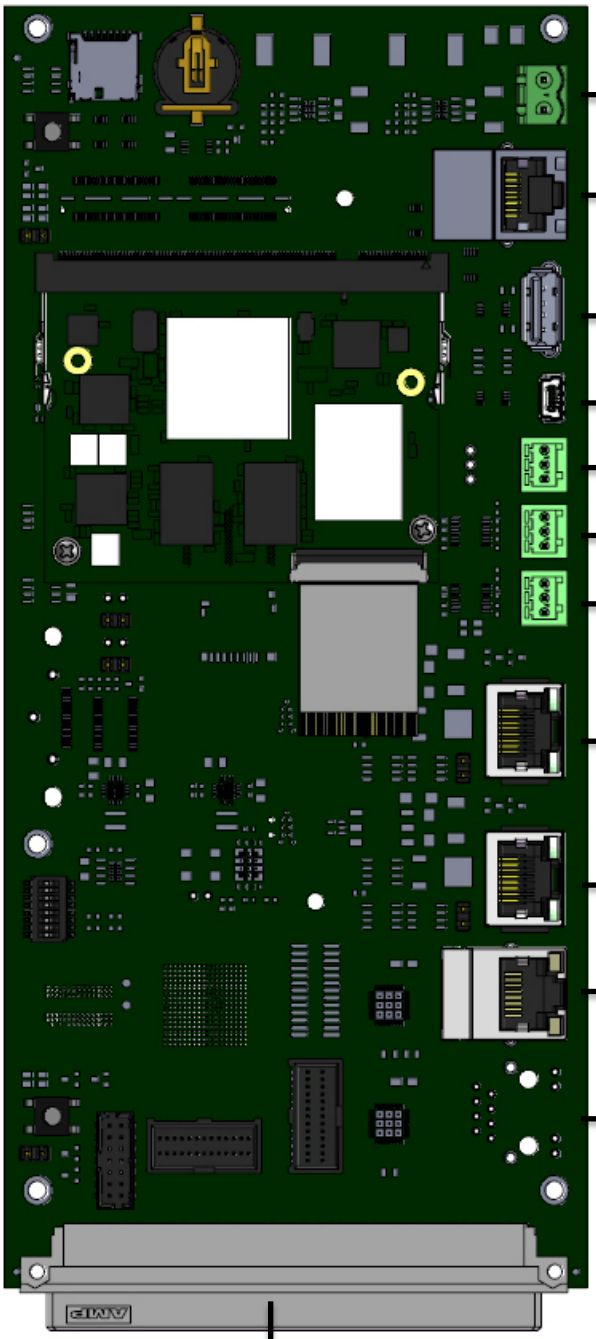
BLOCK DIAGRAM AND SPECIFICATIONS



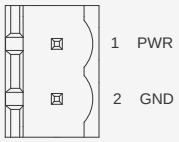
Power Specifications		
Description	Units	Value
DC Supply Voltage	VDC	24 (±25 %)
Control Specifications		
Description	Units	Value
Network Communication Interfaces	-	CANopen, EtherCAT, Ethernet Powerlink, RS232
Ethernet Connectivity	-	10 / 100 / 1000 Mbps Ethernet with Auto MDI/MDIX
USB Connectivity	-	USB 2.0 OTG (supports 480 Mbps and 12 Mbps speed devices), USB 2.0 (supports 480 Mbps speed devices – external USB hub required for 12Mbps or 1.5 Mbps speed devices)
Number of Axes Supported	-	Field-bus dependent
Motors Supported	-	Closed Loop Vector, Single Phase (Brushed, Voice Coil, Inductive Load), Three Phase (Brushless)
System on Module	-	Variscite VAR-SOM-MX6
System On Module Clock (max)	GHz	1.2
System On Module RAM	MB	256 – 2048 DDR3
System On Module Core	-	ARM Cortex-A9
FPGA	-	Xilinx® Spartan®-6 (default XC6SLX25-2CSG324C)
Mechanical Specifications		
Description	Units	Value
Agency Approvals	-	UL Pending, cUL Pending, CE Pending, RoHS II
Size (H x W x D)	mm (in)	227.28 x 99.95 x 16.97 (8.95 x 3.94 x 0.67)
Weight	g (oz)	TBD
Operating Temperature Range	°C (°F)	0 - 75 (32 - 167)
Storage Temperature Range	°C (°F)	-40 - 85 (-40 - 185)
ETHERNET COMM Connector	-	Shielded RJ-45 socket
USB 2.0 COMM Connector	-	Vertical mount USB port
USB 2.0 OTG COMM Connector	-	5-pin, Mini USB B Type port
AUX TERMINAL SERIAL Connector	-	3-pin, 2.5 mm spaced, enclosed, friction lock header
RS232 COMM Connector	-	3-pin, 2.5 mm spaced, enclosed, friction lock header
CANOPEN COMM Connectors	-	Shielded dual RJ-45 sockets
ETHERCAT/ETHERNET COMM Connectors	-	Shielded dual RJ-45 sockets
I/O Connector	-	96-pin, 2.54 mm spaced plug connector
POWER Connector	-	2-port, 5.08 mm spaced, enclosed, friction lock header

Information on Approvals and Compliances	
RoHS II Compliant	The RoHS II Directive 2011/65/EU restricts the use of certain substances including lead, mercury, cadmium, hexavalent chromium and halogenated flame retardants PBB and PBDE in electronic equipment.

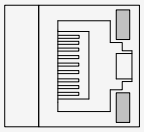
CONNECTOR INFORMATION



P1 - Power Connector
- 2-pin, 5.08mm spaced enclosed friction lock header
- 24 VDC Power Supply Connection
- Mating Connector Included (Phoenix Contact: P/N 1757019)



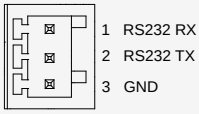
P2 - Ethernet Connector
- Single RJ45 Plug
- 10/100/1000 Mbps Ethernet with auto MDI/MDI-X
- Uses standard CAT 5e or CAT 6 Cable



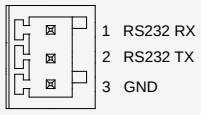
P3 - USB 2.0 Host Connector
- Vertical-mount USB port
- High (480 Mbps) speed devices
- Uses standard USB cable

P4 - USB 2.0 OTG Connector
- 5-pin, Mini USB B Type port
- High (480 Mbps) and Full (12 Mbps) speed devices
- Uses standard USB to MINI-B ASSY cable

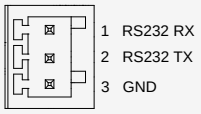
P6 - RS232 Communication Connector
- 3-pin, 2.5mm spaced enclosed friction lock header
- Drive Communication
- Mating Connector Included (Phoenix Contact: P/N 1881338)



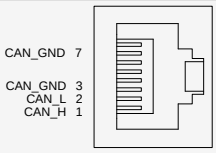
P5 - Aux Terminal Connector
- 3-pin, 2.5mm spaced enclosed friction lock header
- Access to the console via a terminal emulator
- Mating Connector Included (Phoenix Contact: P/N 1881338)



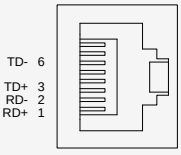
P7 - FPGA RS232 Communication Connector
- 3-pin, 2.5mm spaced enclosed friction lock header
- RS232 connection to the FPGA
- Mating Connector Included (Phoenix Contact: P/N 1881338)



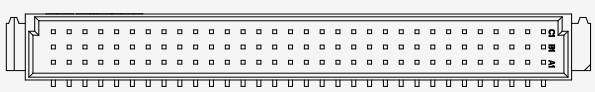
P8 and P9 - CAN Connectors
- Single or Dual RJ45 Plugs
- Uses standard CAT 5e or CAT 6 Cable



P10 and P11 - EtherCAT / Ethernet Connectors
- Single or Dual RJ45 Plugs
- Uses standard CAT 5e or CAT 6 Cable



P12 - I/O Module Connector
- 96-pin, 2.54mm spaced plug connector
- Optional external I/O Module interface

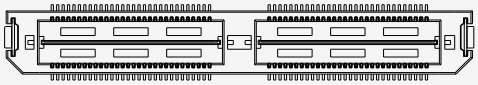


ONNECTOR INFORMATION (CONT.)

P22 and P28 - Micro SD Card Slots
- P28 optional
- Standard removable SD card socket
- Direct connection to the SOM and FPGA

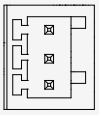
Optional Real Time Clock Backup Battery Holder
- Holds a CR1220 (3V Lithium) battery

P27 - Optional External Devices Connector
- Camera, PCIe, SATA, analog and digital audio interface



P20 - SOM Module Connector

P15 - RS232 Communication Hardware Flow Control
- Optional Connector
- 3-pin, 2.5mm spaced enclosed friction lock header
- Contains the RTS and CTS flow control signals of serial port P6
- Mating Connector Included (Phoenix Contact: P/N 1881338)



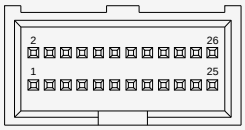
P21 - Auxiliary SOM Connector
- Primary interface between the ARM and the FPGA

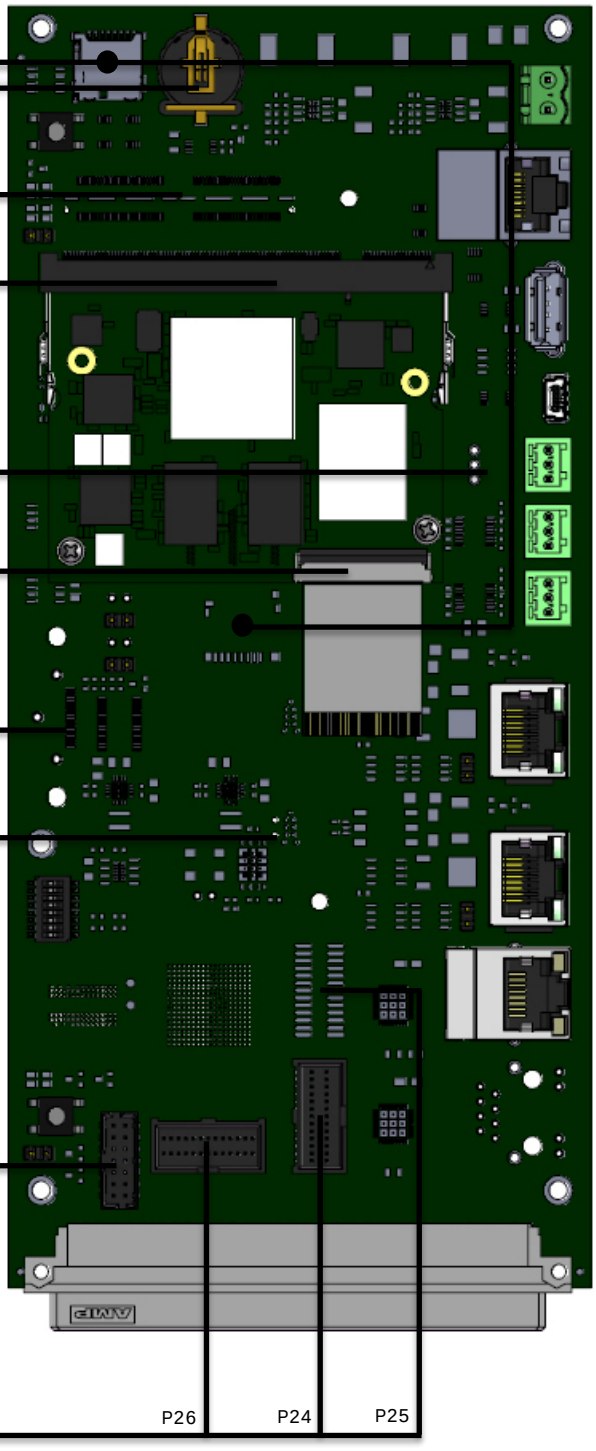
P14 - HDMI Connector

P23 - Optional FPGA SPI FLASH Interface Connector

JTAG1 - FPGA JTAG Connector
- 14-pin, dual row board-to-board header
- Connects to Standard Xilinx Platform Cable USB Ribbon Cable

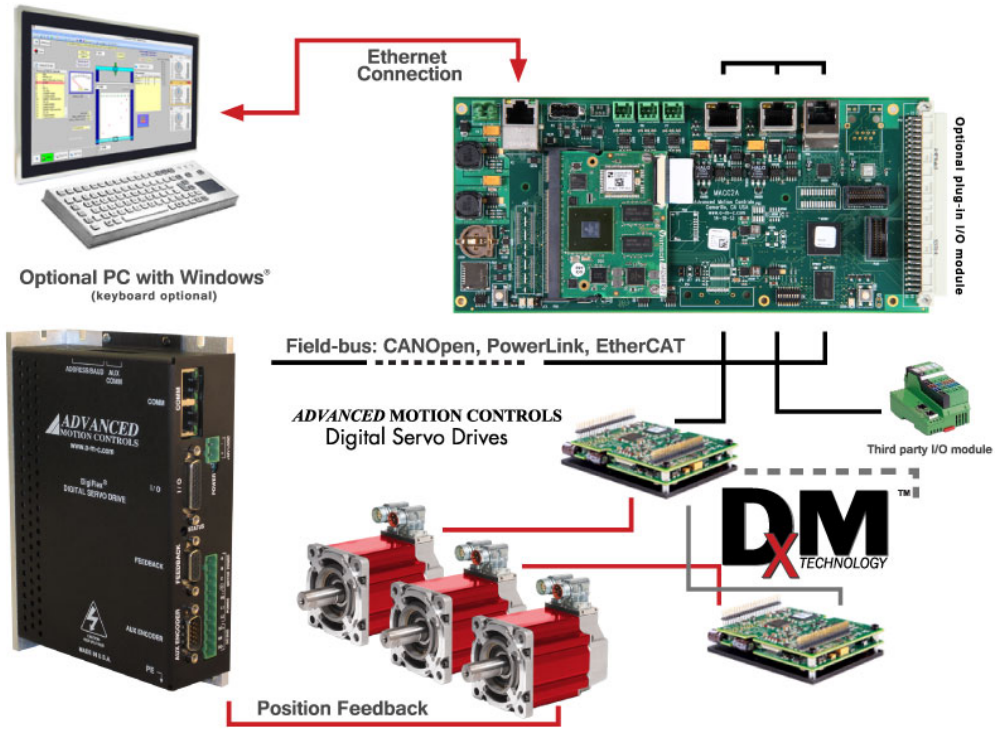
P24, P25, and P26 - Auxiliary FPGA I/O Connectors
- P25 optional
- Mating Connector (Samtec:P/N RSM-113-02-L-D or SMS-113-01-L-D)





MACC SYSTEM CONFIGURATIONS

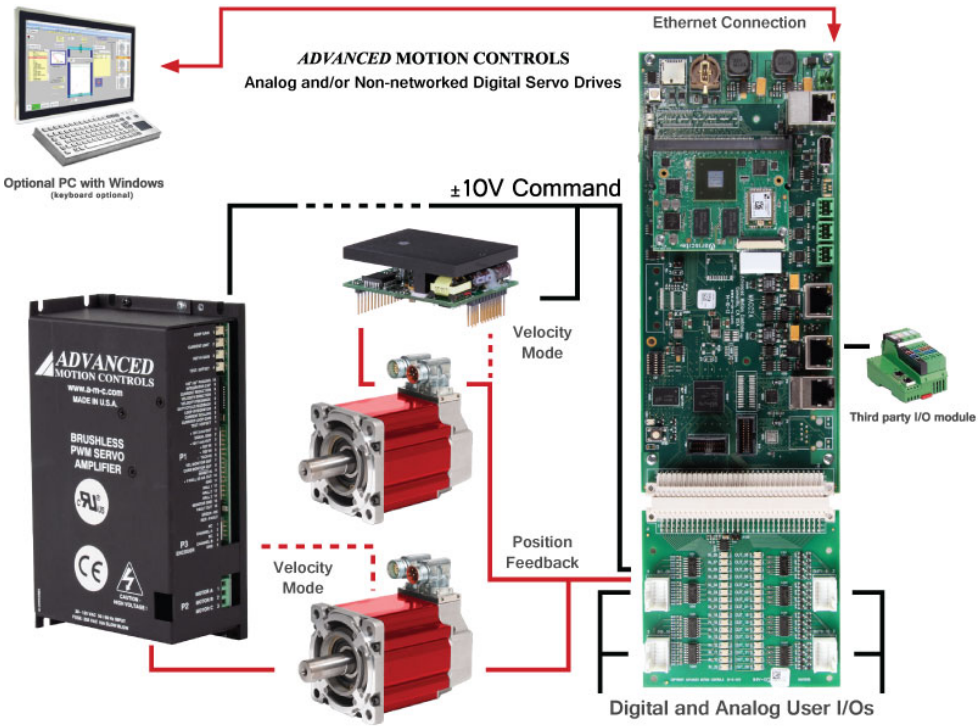
MACC02 with Network Drives and I/O Module



This solution can meet demands for drive and I/O command update rates in the few hundred microseconds range. The MACC integrates field bus masters, such as EtherCAT, CANopen, or Ethernet Powerlink (EPL), directly or they can be installed into an external PC.

To lower drive system costs, *ADVANCED* Motion Controls' exclusive DxM Technology can be utilized. Using only one EtherCAT drive, other sub-nodes could be readily connected.

MACC02 with Torque or Velocity Mode Drives



The analog outputs of the plug-in I/O module of the MACC are connected to the ±10V input of torque or velocity mode drives. Non-networked servo drives, combined with the MACC, provide a system with the lowest overall cost.

This solution can meet demands for drive and I/O command update rates in the 50 microsecond range. However, due to noise and wiring considerations, cable length between the drives/motors and the controller is limited to within a few meters. In this case, motor feedback connections are made to the external I/O module's dedicated inputs.

To provide additional I/Os, pins of the MACC's FPGA are buffered and brought out to an optional connector which can be used by a plug-in I/O expansion card with an SSI (synchronous serial interface).

HARDWARE SETTINGS

Switch Functions

Switch	Description
BTN1	Hardware Reset - automatic system reboot.
BTN2	Manual FPGA configuration clear. If JF4 is installed, will also reboot from the on-board SPI FLASH.
Switch	**Description**
SW1	8-position user-defined DIP Switch (access to 4 DIP Switches through the FPGA)

Note: DIPSW7 controls the SD card and FPGA serial programming interface operation. When this switch is OFF, both the SD card and the serial FPGA programming interface are controlled by the SOM module. When this switch is ON during Linux kernel boot-up, the SD card and serial FPGA programming hardware interface in the SOM module are turned off. The hardware pins are in a high impedance state.

Note: DIPSW8 controls the Bluetooth and WLAN device operation. When it is in the OFF state during system boot-up, the Bluetooth and WLAN device will not be started. DIPSW8 needs to be set to the ON state before power-up to enable the WLAN device, the Bluetooth device, and Bluetooth services.

MACC LED Functions

LED	Description
LED1	Status Bi-color LED. Solid red during boot-up. Blinking red when system load is complete. Green functionality is user-defined through the ARM.
LED2	Bi-color LED. User-defined functionality through the FPGA.
LED3	Power Supply Bi-color LED. Red LED indicates the internal +5V power supply is operational. Green LED indicates that the system reset signal is inactive, and the system is running.
LED4	Status Bi-color LED of the optional FPGA boot microcontroller. For more information refer to the FPGA Boot Options section.

Jumper Settings

Jumper	Description	Configuration	
	Header Jumper	Not Installed*	Installed
JF1	CAN1 bus termination.	Non-terminating node	Terminating node
JF2	CAN2 bus termination	Non-terminating node	Terminating node
JF3	ARM Boot Select**	On-board NAND FLASH	SD Card
JF4	FPGA Boot Mode	Slave Serial Boot	On-board SPI FLASH
JF5	FPGA Configuration Clear on System Reset	No operation	Clear FPGA on reset
JF6	Board EEPROM Write Enable	Disabled	Enabled
JF7	FPGA EEPROM Write Disable	Enabled	Disabled
JF8	FPGA EEPROM A1 Address Bit	Low	High
JF9	Disable hardware watchdog	Watchdog enabled	Watchdog disabled

*Default

** The ARM Boot Select signal is shared with the EIM_DA7 ARM External Interface Module signal. For more information refer to the “ARM External Interface Module Signals” section.

CAN Connector LED Functions

LED	Description
Yellow	Displays the dominant bits (traffic) on the bus
Green	Displays the traffic generated by the MACC02

Hardware Watchdog Circuit

A watchdog is a timer circuit that can generate a hardware event if it has not been triggered within the specified timeout time. For the MACC02, the timeout time is about 1.2 seconds. The MACC watchdog has two functions. The first is a system boot-up guard. In this mode, the watchdog circuit generates a reset event to the system if the Linux serial terminal does not generate any message within the timeout time (e.g. the boot loader locked up). The Linux serial terminal data disables the watchdog. As a secondary function, the watchdog can be used as a hardware watchdog (for generating a system reset event if no trigger occurs within the timeout period) during your application runtime. The circuit will need to be re-enabled via the SOM module GPIO output. The trigger signal is the FPGA_CFG_DATA hardware signal. The signal can be generated as a SOM module GPIO, or as a signal output of the FPGA. This is an optional feature. Contact *ADVANCED* Motion Controls for the availability of this option.

Real Time Clock (RTC) Multiplexer

The on-board RTC can be shared between the SOM module (e.g. the Linux system) and the FPGA. By default, once the SOM has finished boot-up and is done with the RTC, it gives exclusive control to the FPGA. To adjust the RTC from the SOM (Linux system) context, exclusive control over the RTC must be taken back. For more information refer to the section ‘Setting the System Clock’.

SOFTWARE SETTINGS

The MACC02 is shipped pre-installed with Linux and Xenomai real-time extension. Applications can be created for the MACC02 using the Click&Move® (C&M) development environment. Please download the latest version of C&M from *ADVANCED* Motion Controls' website (www.a-m-c.com).

Terminal Console

A serial port on a PC and a terminal program (i.e. *putty*) can be connected to P5 (Aux Terminal Connector) on the MACC02. It is the local serial terminal of the operating system. (Serial terminal settings: 115200,8,1, no parity, no flow control) Use the following user name and password to log in:

User name: **root**
Password: **password**

Telnet Server

Log in to the telnet server of the MACC02 using a remote terminal (*putty*, for example) at TCP port 23 using the same user name and password as used for the serial terminal.

FTP Server

There is an FTP server available on the MACC02. Files can be downloaded to/from the MACC02 using an FTP client (i.e. *Filezilla*). FTP login credentials:

192.168.100.50:21
User: **root**
Password: **password**

Ethernet IP Address

The default network settings of the main (P2) Ethernet interface (eth0) are the following:

IP Address: **192.168.100.50**
Netmask: **255.255.255.0**

These settings can be changed by editing the */etc/network/interfaces* file of the MACC02. Obtain the file using an FTP client, modify it, and then update the existing file in the hardware. The new settings will be available after the MACC02 is rebooted.

WLAN

If DIPSW8 is set to the ON state during boot-up, the WLAN interface is turned on. List the available networks by entering the following command into the terminal console or to a remote telnet terminal window:

```
iwlist wlan0 scan
```

To connect to an encrypted network, find the network from the above list.

```
wpa_passphrase <YourAP> <YourPassword> >wpa.conf
ps | grep wpa_supplicant     // kill the wpa_supplicant process if it exists
wpa_supplicant –Dwext –iwlan0 –c./wpa.conf -B
udhcp –iwlan0
ifconfig
```

External Media

A USB device plugged into the USB host (P3) connector will be auto-mounted under */media/sda1*. An SD Card inserted into the microSD card slot (P22) will be auto-mounted under */media/mmcblk0p1*.

Secondary ethernet interfaces can be added to the MACC02 by connecting USB ethernet adapter(s) to the USB host (P3) connector. If the device is available at boot-up, the default IP address of the second and third ethernet devices will be set by the kernel according to the following table:

eth1: IP address: 192.168.101.50
Netmask: 255.255.255.0
eth2: IP address: 192.168.102.50
Netmask: 255.255.255.0

The supported devices are:
ASIx Ax88772
Moschip 7830/7832/7730

Setting the System Clock

The system time can be set by typing the following into the terminal console:

```
date ––set="2013-11-20 14:58:00"
```

The hardware clock can be set to the current system time as follows:

```
hwclock –w
```

If a battery backup is installed, this will only need to be done once.

Note: Since the FPGA has exclusive control over the hardware clock (RTC) after system boot-up, you must take it back before executing the 'hwclock' command. This can be accomplished by setting a GPIO to logic high using this command:

```
echo 1 > /sys/class/gpio/gpio146/value
```

Exclusive control can be returned to the FPGA using this command:

```
echo 0 > /sys/class/gpio/gpio146/value
```

Using the NAND Recovery Image

ADVANCED Motion Controls provides a recovery SD card image that can be used to install the pre-build U-Boot, Linux kernel, and UBI file system as an easy and fast way to recover the NAND flash. Access to the local serial terminal (P5) of the MACC02 is required during this procedure.

Preparing a recovery card:

LINUX:

- Plug in an SD card (at least 4GB) to your Linux host machine, run dmesg command and see what device is added (i.e. /dev/sdX)
- tar xjvf macc02b-amc-nand-recovery-sd.v1.img.bz2 (contact *ADVANCED* Motion Controls for availability)
- dd if= macc02b-amc-nand-recovery-sd.v1.img of=dev/sdX bs=128k

WINDOWS:

- Use Winrar (http://www.win-rar.com/start.html?&L=0) to unpack the macc02b-amc-nand-recovery-sd.v1.img.bz2 file.
- Download and install USB Writer (http://sourceforge.net/p/usbwriter/wiki/Documentation/) or any similar tool that can write a binary image onto a USB-based device.
- Plug in an SD card (at least 4GB) to your PC using a USB-based SD card reader and run the USBWriter tool. Select the unpacked image file as source file. Select your SD card as Target device.

Recover the NAND flash:

- Insert the SD card into the SD card slot (P22) of the MACC02
- Connect a serial terminal to P5
- Power up the MACC
- Stop the booting procedure in the bootloader. In the U-Boot prompt, enter: "nand erase"
- Install JF3, and power-cycle the MACC02 – this will boot from the recovery SD card
- After a short booting period, LED1 will alternate between red and green, indicating that the FLASH operation is in progress. At the end of a successful recovery operation, the green LED should begin blinking.
- Power down the MACC02, remove the SD card, remove JF3, and power up the MACC02 again.

FPGA I/O INFORMATION

FPGA Auxiliary Power Supply

The auxiliary power supply of the FPGA is 3.3V. The following line must be specified in the UCF file of the FPGA project to indicate this fact to the compiler:

```
CONFIG VCCAUX=3.3;
```

For more information refer to the "Supply Voltages for the IOBs" section of the UG381 User's Guide from Xilinx. (http://www.xilinx.com/support/documentation/user_guides/ug381.pdf)

Bitfile Generation for Slave Serial Download

Change the default configuration startup clock setting from JTAGCLK to CCLK. Make sure to have this line in the *etc\bitgen.ut* file of the Xilinx EDK project:

```
-g StartUpClk:CCLK
```

Main FPGA I/O Connector Pinout

Note that the pin labels on the silkscreen correspond to the connector labels as such:
Pins 1-32 = C1-C32; Pins 33-64 = B1-B32; Pins 65-96 = A1-A32

P12 – Main FPGA I/O Connector

Pin	Description/Notes	FPGA Ball	Pin	Description/Notes	FPGA Ball	Pin	Description/Notes	FPGA Ball
1	I/O	J6	33	I/O	J7	65	+POWER_IN	-
2	I/O	J1	34	I/O	J3	66	+POWER_IN	-
3	I/O	H6	35	I/O	H7	67	+POWER_IN	-
4	I/O	H4	36	I/O	H5	68	GND	-
5	I/O	H1	37	I/O	H2	69	GND	-
6	I/O	G1	38	I/O	G3	70	I/O	H3
7	I/O	F5	39	I/O	F6	71	I/O	G6
8	I/O	F2	40	I/O	F3	72	I/O	F4
9	I/O	E3	41	I/O	E4	73	I/O	F1
10	I/O	D2	42	I/O	D3	74	I/O	E1
11	I/O	C1	43	I/O	C2	75	I/O	D1
12	I/O	A3	44	I/O	A2	76	I/O	B2
13	I/O	B3	45	I/O	A4	77	GND	-
14	I/O	B4	46	I/O	C4	78	GND	-
15	I/O	A5	47	I/O	C5	79	GND	-
16	I/O	A6	48	I/O	B6	80	GND	-
17	I/O	C6	49	I/O	D6	81	GND	-
18	I/O	A7	50	I/O	C7	82	I2C_SCL	-
19	I/O	A8	51	I/O	B8	83	I2C_SDA	-
20	I/O	C8	52	I/O	D8	84	RESET	-
21	I/O	A9	53	I/O	B9	85	GND	-
22	I/O	C9	54	I/O	D9	86	GND	-
23	I/O	F9	55	I/O	G9	87	+3.3V	-
24	I/O	A10	56	I/O	C10	88	+3.3V	-
25	I/O	A11	57	I/O	B11	89	GND	-
26	I/O	C11	58	I/O	D11	90	GND	-
27	I/O	A12	59	I/O	B12	91	+3.3V	-
28	I/O	E13	60	I/O	F13	92	+3.3V	-
29	I/O	A14	61	I/O	B14	93	GND	-
30	I/O	C14	62	I/O	D14	94	GND	-
31	I/O	A15	63	I/O	C15	95	+5V	-
32	I/O	A16	64	I/O	B16	96	+5V	-

Auxiliary FPGA I/O Connector Pinouts

P24 – Auxiliary I/O Connector

Pin	Description/Notes	FPGA Ball	No Connect[1]	Pin	Description/Notes	FPGA Ball	No Connect[1]
1	I/O	K1	-	14	I/O	M1	-
2	I/O	K2	-	15	I/O	M3	-
3	I/O	K3	-	16	I/O	N4	-
4	I/O	K4	-	17	I/O	N5	-
5	I/O	K5	-	18	I/O; Note 2	V3	-
6	I/O	K6	-	19	I/O	P8	LX9
7	I/O	L1	-	20	I/O; Note 2	T13	-
8	I/O	L2	-	21	I/O	N7	LX9
9	I/O	L3	-	22	+3.3V	-	-
10	I/O	L4	-	23	GND	-	-
11	I/O	L5	-	24	GND	-	-
12	I/O	L6	-	25	GND	-	-
13	I/O	L7	-	26	GND	-	-

Note 1: The No Connect column indicates which FPGA device option does not have the signal on the connected ball.

Note 2: If the SPI FLASH is the FPGA configuration source, these signals are outputs and active during the configuration procedure. These signals should be configured in the design only as inputs, or not used at all.

P25 – Optional Auxiliary I/O Connector

Pin	Description/Notes	FPGA Ball	No Connect[1]	Pin	Description/Notes	FPGA Ball	No Connect[1]
1	I/O	P1	-	14	I/O	U2	-
2	I/O	P2	-	15	I/O	U5	-
3	I/O	P3	-	16	I/O; Note 2	N1	-
4	I/O	P4	-	17	I/O; Note 2	N2	-
5	I/O	P6	-	18	I/O; Note 2	N3	-
6	I/O	R3	-	19	I/O	V4	-
7	I/O	R5	-	20	I/O	V5	-
8	I/O	T1	-	21	I/O	V6	-
9	I/O	T2	-	22	I/O	N8	LX9
10	I/O	T3	-	23	I/O	T6	-
11	I/O	T4	-	24	I/O	M8	LX9
12	I/O	T5	-	25	+3.3V	-	-
13	I/O	U1	-	26	GND	-	-

Note 1: The No Connect column indicates which FPGA device option does not have the signal on the connected ball.

Note 2: These signals are available only if both connectors P24 and P25 are available (e.g. if both Ethernet PHY for the FPGA are uninstalled). Do not connect any signal to these pins if only P25 is available.

P26 – Auxiliary I/O Connector

Pin	Description/Notes	FPGA Ball	No Connect[1]	Pin	Description/Notes	FPGA Ball	No Connect[1]
1	FPGA_I2C_SDA; Note 2	A13	LX9	14	I/O	E11	LX9, LX45
2	FPGA_I2C_SCL; Note 2	C13	LX9	15	GND	-	-
3	I/O	F12	LX9, LX45	16	I/O	F10	LX9, LX45
4	I/O	E12	LX9, LX45	17	GND	-	-
5	+3.3V	-	-	18	I/O	G8	LX9, LX25, LX45
6	I/O	D12	LX9, LX45	19	GND	-	-
7	+3.3V	-	-	20	I/O	F8	LX9, LX25, LX45
8	I/O	C12	LX9, LX45	21	GND	-	-
9	+3.3V	-	-	22	I/O	E8	LX9, LX25, LX45
10	I/O	G11	LX9, LX45	23	OUT; Note 3	D4	-
11	GND	-	-	24	I/O	F7	LX9, LX25, LX45
12	I/O	F11	LX9, LX45	25	I/O	E6	LX9, LX25, LX45
13	GND	-	-	26	I/O	E7	LX9, LX25, LX45

Note 1: The No Connect column indicates which FPGA device option does not have the signal on the connected ball.

Note 2: The FPGA_I2C signals are connected to the on-board user EEPROM. The default device is 24C64.

Note 3: Pin 23 is connected to the HSWAPEN FPGA pin. It needs to be floating, to disable weak pull-ups to all FPGA pins before FPGA configuration. Pin 23 should be used for output purposes only.

Additional FPGA Signals

Certain FPGA pins have predefined functionality. Configure these pins according to the following tables.

Signal	FPGA Ball	Dir[1]	Functionality
FPGA_CFG_INIT	U3	I/O	Open drain output during configuration. Use as I/O after configuration. ARM GPIO_104, or SPI1_DIN. Optional RTC multiplexer selector signal.
FPGA_CFG_CLK	R15	I	Serial clock input during configuration. Use as input after configuration. ARM SPI1_CLK.
FPGA_CFG_DATA	R13	I	Serial data input during configuration. Use as input after configuration. ARM SPI1_DOUT. Optional hardware watchdog trigger signal.
FPGA_STATUS1	U16	I/O	User I/O between ARM and FPGA. ARM GPIO_83.
FPGA_STATUS2	V16	I/O	User I/O between ARM and FPGA. ARM GPIO_84.
FPGA_STATUS3	N6	I/O	(No Connect on LX9) User I/O between ARM and FPGA (ARM GPIO_21), or FPGA_UART_PHY_TX (available on P7).
FPGA_STATUS4	P7	I/O	(No Connect on LX9) User I/O between ARM and FPGA (ARM GPIO_20), or FPGA_UART_PHY_RX (available on P7).
FPGA_UART_TX	U15	O	(No Connect on LX9) ARM UART3_RX.
FPGA_UART_RX	V15	I	(No Connect on LX9) ARM UART3_TX.
!SYS_RST	V14	I	Active low system reset signal.
SYS_CLK	V10	I	50MHz clock input. Note 2.
LED_RED	L14	O	User defined FPGA status LED.
LED_GREEN	M13	O	User defined FPGA status LED.
DIPSW0	F14	I	DIPSW input.
DIPSW1	C18	I	DIPSW input.
DIPSW2	P16	I	DIPSW input.
DIPSW3	P15	I	DIPSW input.
PS_SYNC	T15	O	Optional 1MHz synchronization clock for on-board DC/DC converters. Shared with M0 configuration mode selector pin. Generate 1MHz 50% duty cycle signal to this output pin, or configure it to input and do not use it.

Note 1: All direction information is from the FPGA point of view.

Note 2: The default clock source for the FPGA is the on-board 50MHz crystal oscillator. However, it is possible to use the clock output of the SOM module instead. This feature is SMD jumper selectable. The frequency of this SOM module clock output is software programmable.

DDR2 RAM Interface

The DDR2 memory device is connected to the FPGA memory controller interface of I/O Bank 1. The standard pin assignment is applied. The default RAM device is Micron MT47H64M16HR-3.

Signal	FPGA Ball	Dir[1]	Signal	FPGA Ball	Dir[1]
DDR_A0	H15	O	DDR_DQ11	P18	I/O
DDR_A1	H16	O	DDR_DQ12	T17	I/O
DDR_A2	F18	O	DDR_DQ13	T18	I/O
DDR_A3	J13	O	DDR_DQ14	U17	I/O
DDR_A4	E18	O	DDR_DQ15	U18	I/O
DDR_A5	L12	O	DDR_BA0	H13	O
DDR_A6	L13	O	DDR_BA1	H14	O
DDR_A7	F17	O	DDR_BA2	K13	O
DDR_A8	H12	O	!DDR_WE	K12	O
DDR_A9	G13	O	!DDR_RAS	K15	O
DDR_A10	E16	O	!DDR_CAS	K16	O
DDR_A11	G14	O	DDR_CKP	G16	O
DDR_A12	D18	O	!DDR_CKN	G18	O
DDR_A13	C17	O	DDR_CKE	D17	O
DDR_DQ0	M16	I/O	DDR_ODT	K14	O
DDR_DQ1	M18	I/O	DDR_LDQSP	K17	I/O
DDR_DQ2	L17	I/O	!DDR_LDQSN	K18	I/O
DDR_DQ3	L18	I/O	DDR_UDQSP	N15	I/O
DDR_DQ4	H17	I/O	!DDR_UDQSN	N16	I/O
DDR_DQ5	H18	I/O	DDR_LDM	L16	O
DDR_DQ6	J16	I/O	DDR_UDM	L15	O
DDR_DQ7	J18	I/O	RZQ	F15	-
DDR_DQ8	N17	I/O	ZIO	M14	-
DDR_DQ9	N18	I/O	VREF	N14, F16	-
DDR_DQ10	P17	I/O			

Note 1: All direction information is from the FPGA point of view.

ARM External Interface Module Signals

This is the primary interface between the ARM and the FPGA. It is a 16-bit synchronous multiplexed address/data bus, with 16 data and 16 address lines.

Signal	FPGA Ball	Dir[1]	Functionality
EIM_BCLK	V9	I	66MHz burst clock. Active only during bus transactions.
!EIM_CS	T14	I	Active low chip select.
!EIM_OE	V13	I	Active low output enable.
!EIM_LBA	U10	I	Active low address valid.
!EIM_RW	V7	I	Active low write enable.
!EIM_EB0	N10	I	(No Connect on LX9) Active low low-byte enable. Active during write operations only.
!EIM_EB1	T12	I	(No Connect on LX9) Active low high-byte enable. Active during write operations only.
EIM_DA0	T9	I/O	Multiplexed address/data signal.
EIM_DA1	V11	I/O	Multiplexed address/data signal.
EIM_DA2	U8	I/O	Multiplexed address/data signal.
EIM_DA3	U13	I/O	Multiplexed address/data signal.
EIM_DA4	R8	I/O	Multiplexed address/data signal.
EIM_DA5	U11	I/O	Multiplexed address/data signal.
EIM_DA6	P12	I/O	Multiplexed address/data signal.
EIM_DA7[2]	T11	I/O	Multiplexed address/data signal.
EIM_DA8	R11	I/O	Multiplexed address/data signal.
EIM_DA9	T8	I/O	Multiplexed address/data signal.
EIM_DA10	R7	I/O	Multiplexed address/data signal.
EIM_DA11	U7	I/O	Multiplexed address/data signal.
EIM_DA12	T10	I/O	Multiplexed address/data signal.
EIM_DA13	T7	I/O	Multiplexed address/data signal.
EIM_DA14	R10	I/O	Multiplexed address/data signal.
EIM_DA15	V8	I/O	Multiplexed address/data signal.

Note 1: All direction information is from the FPGA point of view.

Note 2: This ARM pin is shared with the ARM Boot Select signal. When JF3 jumper is installed, it forces this signal to logic low. Note that the ARM to FPGA bus will not work properly this way. This is important when the system is booted from the SD card instead of the on-board NAND FLASH.

Micro SD Card Interface

The primary SD card slot (P22) is shared between the ARM and the FPGA. After system bootup the MMC master is the ARM. The ARM can grant access to the resource for another MMC master. The procedure is accomplished by a handshaking mechanism, using the FPGA_STATUS1 and FPGA_STATUS2 signals. Do not drive any of the SD card interface signals from the FPGA while sampling FPGA_STATUS1 signal low. This means the ARM is the owner (the master) of the interface. Indicate that the FPGA is the master by setting FPGA_STATUS2 signal to high. Check the Click&Move® example project *MACCTest* for further information. Optionally, the FPGA can boot directly from this SD card. In this case the optional microcontroller has to be installed. For more information refer to the 'FPGA Boot Options' section in this document. Contact *ADVANCED* Motion Controls for the availability of this option.

Signal	FPGA Ball	Dir[1]	Functionality
SD_CLK	N9	O	(No Connect on LX9) MMC/SD interface clock.
SD_CMD	M11	O	(No Connect on LX9) MMC/SD interface command.
SD_DAT0	V12	I/O	(No Connect on LX9) MMC/SD interface Data0.
SD_DAT1	N11	I/O	(No Connect on LX9) MMC/SD interface Data1.
SD_DAT2	P11	I/O	(No Connect on LX9) MMC/SD interface Data2.
SD_DAT3	M10	I/O	(No Connect on LX9) MMC/SD interface Data3.

Note 1: All direction information is from the FPGA point of view.

P28 (optional micro SD card slot) will be installed only if the application needs a dedicated microSD card slot both for the FPGA and the ARM. If P28 is installed, P22 is isolated from the FPGA using SMD jumpers. P22 will be dedicated to the ARM, while P28 will be dedicated to the FPGA.

Ethernet PHY Interface Signals

For signal descriptions, refer to the datasheet of the DP83848K device.

When a PHY is not installed, the signals are available on the P25 and P24 auxiliary I/O connectors.

Primary PHY				Secondary PHY			
Signal	**FPGA Ball**	**Dir[1]**	**Functionality**	**Signal**	**FPGA Ball**	**Dir[1]**	**Functionality**
OUT_TXCLK	R3	I	-	IN_TXCLK	K6	I	-
OUT_TXEN	P6	O	-	IN_TXEN	K5	O	-
OUT_TXD0	P4	O	-	IN_TXD0	K4	O	-
OUT_TXD1	P3	O	-	IN_TXD1	K3	O	-
OUT_TXD2	P2	O	-	IN_TXD2	K2	O	-
OUT_TXD3	P1	O	-	IN_TXD3	K1	O	-
OUT_RXCLK	U5	I	-	IN_RXCLK	M3	I	-
OUT_RXDV	U2	I	-	IN_RXDV	M1	I	-
OUT_RXER	T5	I	-	IN_RXER	L6	I	-
OUT_RXD0	T3	I	-	IN_RXD0	L4	I	-
OUT_RXD1	T2	I	-	IN_RXD1	L3	I	-
OUT_RXD2	T1	I	-	IN_RXD2	L2	I	-
OUT_RXD3	R5	I	-	IN_RXD3	L1	I	-
OUT_COL	T4	I	-	IN_COL	L5	I	-
OUT_CRS	U1	I	-	IN_CRS	L7	I	-
PHY_CLK	M5	O	Note 2	PHY_CLK	M5	O	Note 2
PHY_MDC	N1	O	Note 2	PHY_MDC	N1	O	Note 2
PHY_MDIO	N2	I/O	Note 2	PHY_MDIO	N2	I/O	Note 2
!PHY_RST	N3	O	Note 2	!PHY_RST	N3	O	Note 2
!OUT_LNK	V4	I	-	!IN_LNK	N4	I	-
!OUT_SPD	V5	I	-	!IN_SPD	N5	I	-
OUT_LED0	M8	O	(No Connect on LX9) Note 3	IN_LED0	N7	O	(No Connect on LX9) Note 3
!OUT_LED0	T6	O	Note 3	!IN_LED0	T13	O	Shared with an SPI mode boot pin. Note 3
OUT_LED1	N8	O	(No Connect on LX9) Note 3	IN_LED1	P8	O	(No Connect on LX9) Note 3
!OUT_LED1	V6	O	Note 3	!IN_LED1	V3	O	Shared with an SPI mode boot pin. Note 3

Note 1: All direction information is from the FPGA point of view.

Note 2: These signals are shared by the two PHY channels.

Note 3: If signal polarity is true, the green LED of the RJ45 will be on. If the signal polarity is false, the red LED will be on. If you are satisfied with the way the PHY controls the LEDs on the !OUT_LNK and !OUT_SPD outputs, you can connect these signals to the !IN_LED0 / !OUT_LED0 and !IN_LED1 / !OUT_LED1 signals inside the FPGA, while pulling IN_LED0 / OUT_LED0 and IN_LED1 / OUT_LED1 signals high. The PHY will control the green LEDs in this way.

FPGA Boot Options

The default boot option of the FPGA is slave serial mode. In this case, the bitfile can be downloaded into the FPGA via the SOM module, using the available Click&Move® (C&M) application development environment function blocks. Refer to the MACCTest C&M example application for details.

Optionally, the FPGA can boot directly from a micro SD or SDHC card, still in slave serial mode. This can be achieved by an optional microcontroller. After power up, the boot loader program of the microcontroller searches for a file in the root of the SD (or SDHC) card file system called 'fpgaboot.txt'. This plain text file should contain the name (with full path) of the FPGA bitfile to use as the boot image. The boot loader supports FAT32 file systems, and can read files and directories with short (old DOS 8.3 naming format) names only. Long file names may be used on the card for files or directories, but in this instance the "alternate file name" must be used for the directory and files names in the fpgaboot.txt file. The alternate files names can be checked using the dir /x command line command. Contact *ADVANCED* Motion Controls for the availability of this option.

The FPGA can be set to SPI boot mode by installing JF4. In SPI boot mode, the FPGA reads the configuration data from the on-board SPI FLASH automatically after power-up. One method of programming the SPI FLASH is explained in this application note from Xilinx: (http://www.xilinx.com/support/documentation/application_notes/xapp974.pdf)

Another method of programming the SPI FLASH is to use the SPI FLASH programming interface connector (P23). This method will require an external SPI master device. A third method is via the SOM module in a similar indirect programming fashion to the Xilinx method. Contact *ADVANCED* Motion Controls for the availability of the latter two methods.

The FPGA can be configured and debugged using the dedicated JTAG interface as well.

Optional FPGA Boot SPI FLASH Programming Connector

All the necessary signals of the SPI FLASH are available at P23. Use a Tag-Connect connector (TC2030-MCP-NL) to access the signals.

P23 – Optional FPGA SPI FLASH Interface Connector

Pin	Signal Name	Dir[1]	Description
1	+3.3V	O	+3.3V output power for the external programming interface
2	SCLK	I	Serial SPI clock
3	SDI	I	Serial data input of the FLASH device
4	!CS	I	SPI bus chip select signal
5	SDO	O	Serial data output of the FLASH device
6	GND	-	Ground

Note 1: All direction information is from the FLASH device point of view.

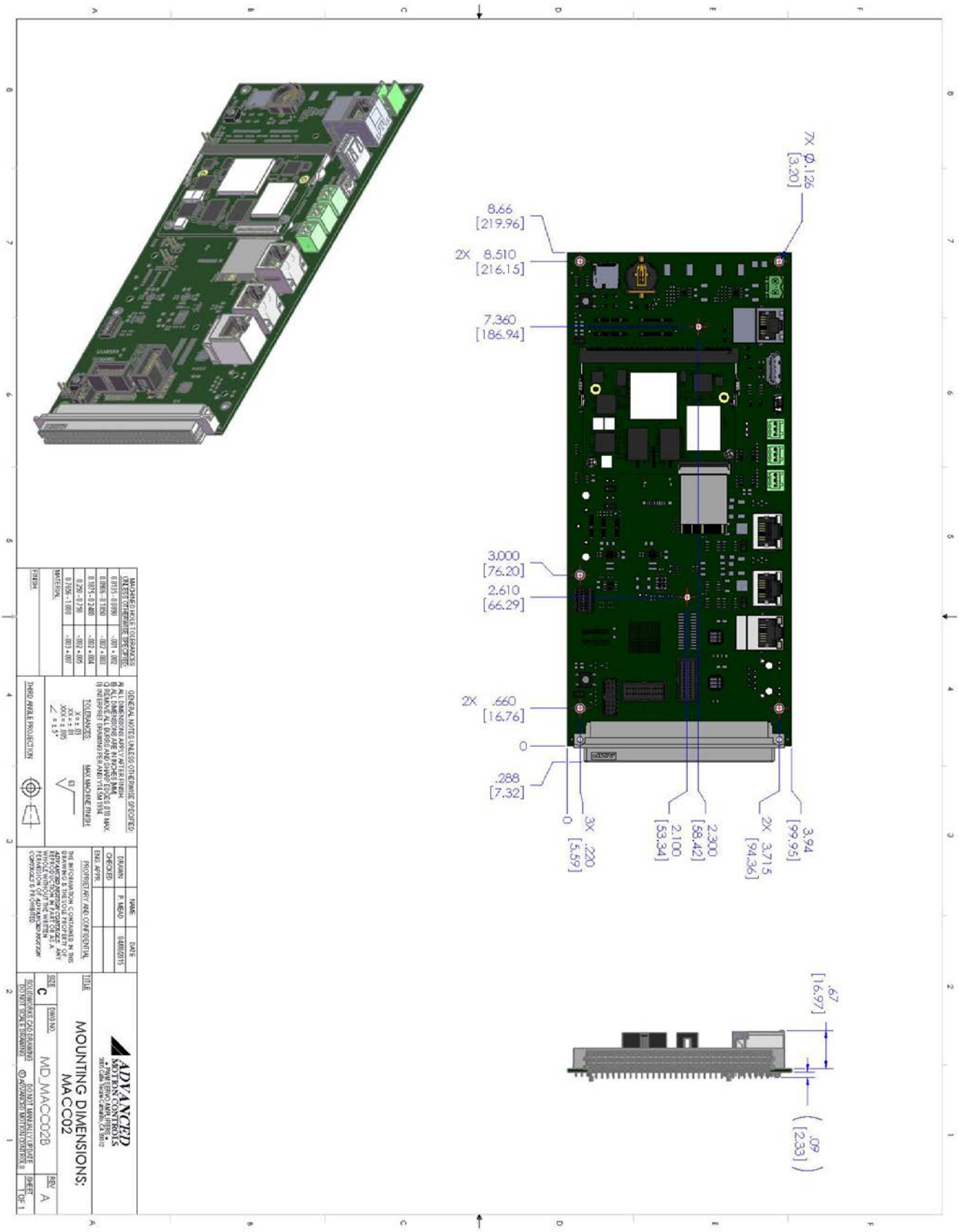
FPGA JTAG Connector

Contains the JTAG signals of the FPGA. The connector is the standard 2mm header that the Xilinx Platform Cable USB JTAG device uses. The standard ribbon cable of the Xilinx device can be used to connect to the MACC02 board.

JTAG1 – FPGA JTAG Connector

Pin	Signal Name	Dir	Description
1	GND	-	Ground
2	+3.3V	O	+3.3V power supply for the external JTAG master
3	GND	-	Ground
4	TMS	I	Test mode select
5	GND	-	Ground
6	TCK	I	Test clock
7	GND	-	Ground
8	TDO	O	Test data output
9	GND	-	Ground
10	TDI	I	Test data input
11	GND	-	Ground
12	NC	-	Not connected
13	GND	-	Ground
14	NC	-	Not connected

MOUNTING DIMENSIONS



CUSTOMIZATION INFORMATION

ADVANCED Motion Controls also has the capability to promptly develop and deliver specified products for OEMs with volume requests. Our Applications and Engineering Departments will work closely with your design team through all stages of development in order to provide the best servo drive solution for your system. Equipped with on-site manufacturing for quick-turn customs capabilities, *ADVANCED* Motion Controls utilizes our years of engineering and manufacturing expertise to decrease your costs and time-to-market while increasing system quality and reliability. Feel free to contact Applications Engineering for further information and details.

Examples of Customized Products

- Optimized Footprint
- Private Label Software
- OEM Specified Connectors
- No Outer Case
- Increased Current Resolution
- Increased Temperature Range
- Custom Control Interface
- Integrated System I/O
- Tailored Project File
- Silkscreen Branding
- Optimized Base Plate
- Increased Current Limits
- Increased Voltage Range
- Conformal Coating
- Multi-Axis Configurations
- Reduced Profile Size and Weight

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